USER´S MANUAL

4M12 COC40™
Version 0.0

08 AUG 1994

For use with:
4MEG VIDEO Model 12

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Image Processing Products
For Research and Industry

Printing: 2 March 1995

1. Installation

The COC40 board is for use with a 4MEG VIDEO Model 12 Revision 4.2 or later revision imaging board. The COC40 will not mount on earlier versions of the Model 12. The term "4MEG VIDEO" or "Model 12" will be used to refer to the 4MEG VIDEO Model 12.

Reference is made to EPIX' 4MIP and 4MIPTOOL software. They will be referred to collectively as 4MIP where differentiation is not required.

1.A Unpacking and Static Warning

The COC40 board is packed in a static dissipative bag. Please keep the bag and box in which the board was shipped, should the need arise to package and return the board.

Prior to opening the bag, place the bag near the PC into which the board will be installed. Touching the bag and the PC should dissipate any static charge that may have been created transporting the board to the PC. A static free area for installation is recommended. Alternatively, use a wrist strap that is connected to the PC.

1.B Connection to Model 12

A connector-extender printed circuit board with two connectors on each side and four standoffs with eight screws attach the COC40 board to the Model 12. The Model 12 must have the image memory board removed prior to the installation of the COC40 board. Plug the connector-extender board onto the Model 12. Mount the 4 standoffs to the Model 12 with the screws provided. Install the COC40 board on top of the Model 12 by plugging the connectors on the back of the COC40 board into the connector-extender that was previously mounted on the Model 12. Install the 4 screws and tighten all 8 screws.

1.C Installation

Remove the brackets and bracket retaining screws from two adjacent 16 bit slots in the PC bus. Check that there is enough clearance to the slot adjacent to the COC40 board.

Plug the two board assembly into two adjacent slots in the PC bus.

Install the required cables.

Turn on the power to the PC and test the boards by running 4MIP and then strobing *Utilities*, *Obscure Menus*, and then *Run Diagnostics*.

2. COC40 Memory

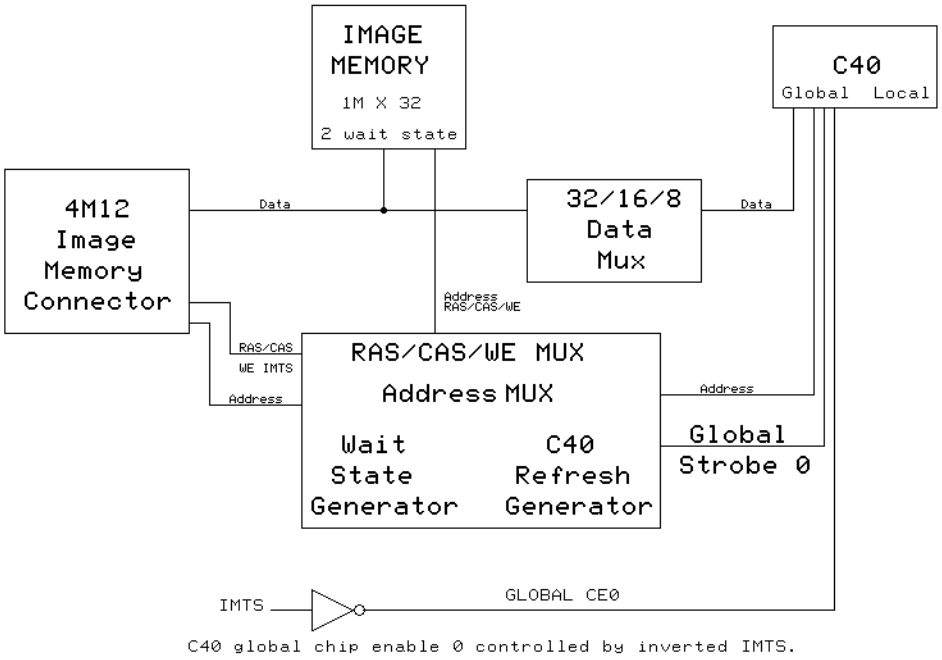

Figure 2-1. COC40 Global Memory

2.A Global Memory

The COC40 has 4 megabytes of dual ported, single access image memory which is shared with the 4MEG VIDEO Model 12 when the Model 12 is connected. Either the Model 12 or the C40 has exclusive access to image memory. Access is controlled by the Image Memory Tri-State bit (IMTS, bit 6) in the T13 register of the Model 12. The IMTS is inverted and connected to the C40 Global Chip Enable 0. The level of the local and global chip enables can be read by the C40. The image memory uses 1M X 4 DRAMs which have a hidden refresh when either the C40 or C25 have access. Two wait states are required for the image memory.

The image memory is accessable as 32 bit words (4 pixels), 16 bit words (2 pixels), or 8 bit bytes (1 pixel) from the global bus of the C40. The global memory space is divided as shown in the table below. Note that on 16 bit and 8 bit reads, the upper 16 or 24 bits, respectively, are forced to zero.

Global Address Bit 30	Global Address Bit 29	Access Type
1	1	32 bit (4 pixels).
1	0	16 bit (2 pixels).
0	1	Reserved.
0	0	8 bit (1 pixel).

TABLE 2-1. C40 Image Memory Width Control

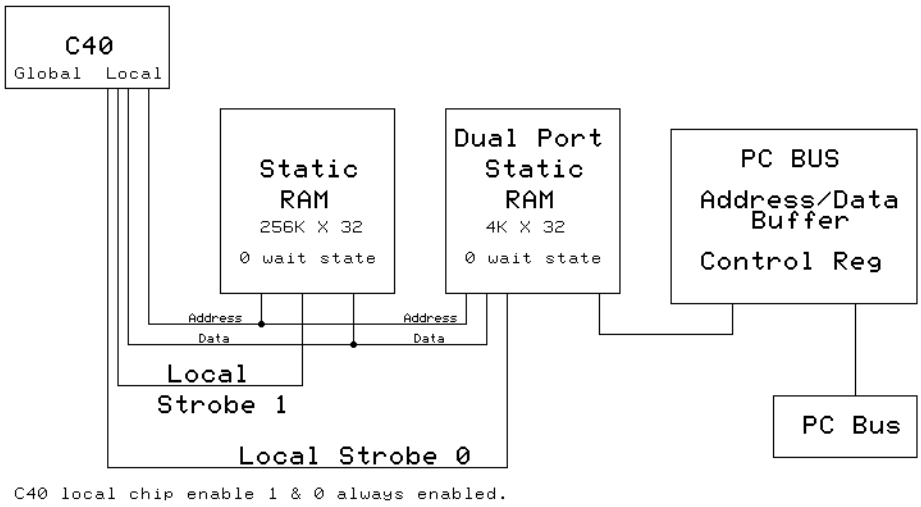

Figure 2-2. COC40 Local Memory

2.B Local Memory

The 4K by 32 bit, zero wait state dual port memory is accessed with the C40's local bus strobe 0. The 256K by 32 bit, zero wait state memory is accessed with the C40's local bus strobe 1. Both the C40's local chip enable 1 and 0 are wired to ground (enabled).

Note that the C40 memory control registers determine the addresses to which the local bus strobes and global bus strobes respond.

2.C Reset Vector

Two jumpers control the starting address after the C40 has been reset. The C40 is reset by the PC on power-up, by the C40GO bit from the Model 12, or by the GOC40 bit from the COC40. The standard jumper configuration is for the starting address at local bus address 0.

Jumper JP1 pins 1&2	Jumper JP1 pins 3&4	Memory Address
no jumper	no jumper	0xFFFF FFFF (global)
no jumper	jumper	0x8000 0000 (global)
jumper	no jumper	0x7FFF FFFF (local)
jumper	jumper	0x0000 0000 (local)

TABLE 2-2. C40 Starting Address Selection Jumpers

3. COC40 PC Bus I/O Control Register

An 8 bit PC Bus I/O register enables PC bus access to the dual port memory, selects the PC bus base address of the dual port memory, selects zero wait state operation of the PC bus access to dual port memory, resets the C40, generates an interrupt to the C40, and indicates when a 4MEG VIDEO Model 12 is connected.

Note that it is not suggested to enable more than one board in the same address space while performing memory reads to the PC bus from that address space. This activity voids the warranty and may create damage one or both board's data buffers.

Bits shown as "RES" are reserved for future use and should be written with zero and masked after a read.

The "I/O" jumper selects either 0x288 or 0x298 as the PC bus I/O register address. The register below is shown with 0x288 as the address. The I/O address decode circuit can be replaced to provide other I/O base selections. The board silkscreen is marked with 0x2A0 or 0x2B0 which correspond to 0x288 or 0x298 respectively.

0x288 C40 and Memory Control Register. Read/Write. Cleared at power up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
M12 NOT CON	RES	C40 NMI	0WS ENB	MEM ADR SEL 1	MEM ADR SEL 0	MEM ENB	GO C40

Bit		7	→	M12 NOT CON (read only)
		1	→	M12 is not connected.
		0	→	M12 is connected.
Bit		5	→	C40 NMI
		1	→	C40 nonmaskable interrupt = 1, generate interrupt.
		0	→	C40 nonmaskable interrupt = 0.
Bit		4	→	0WS ENB
		1	→	PC memory access will be zero wait state.
		0	→	PC memory access will be standard.
Bit	3	2	→	MEM ADR SEL 1,0
	1	1	→	PC memory address decode starting at 0x800000.
	1	0	→	PC memory address decode starting at 0xE00000.
	0	1	→	PC memory address decode starting at 0xE0000.
	0	0	→	PC memory address decode starting at 0xD0000.
Bit		1	→	MEM ENB
		1	→	Selected PC memory access allowed.
		0	→	PC memory access not allowed.
Bit		0	→	GOC40
		1	→	C40 executes instructions.
		0	→	Reset C40.

The M12 NOT CON bit is a read only indicator that a Model 12 is not connected. This bit indicates if image memory arbitration and communication with the Model 12 is required.

The GOC40 bit is logically "ored" with the Model 12 C40GO bit. The C40GO bit from the Model 12 is pulled up on the COC40 so that the C40 will not be reset if the Model 12 is not connected.

4. COC40 Communication Ports

4.A Communication Port 5

Communication port 5 may be connected via a short cable to the 4MEG VIDEO Model 12.

A via allows selection of the Model 12 processor clock or the COC40 clock. The factory selection is for the COC40 clock to be used as the C40 processor clock.

5. LIMITED WARRANTY

EPIX, Inc. warrants the 4MEG VIDEO Model 12 and the COC40 to be in good working order for a period of one year from the date of purchase from EPIX or from an authorized EPIX distributor. Should this product fail to be in good working order at any time during the one year warranty period, EPIX will, at its option, repair or replace this product at no additional charge except as set forth below. Repair parts and replacement Products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of EPIX.

This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse, or non-EPIX modification of the product.

Limited Warranty service may be obtained by delivering the product during the one year warranty period to an authorized EPIX distributor or to EPIX and providing proof of purchase date. If this product is delivered by mail, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location and to use the original shipping container or equivalent. Contact an authorized EPIX distributor or EPIX for further information.

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